

When using this system, the user should be aware of the following:

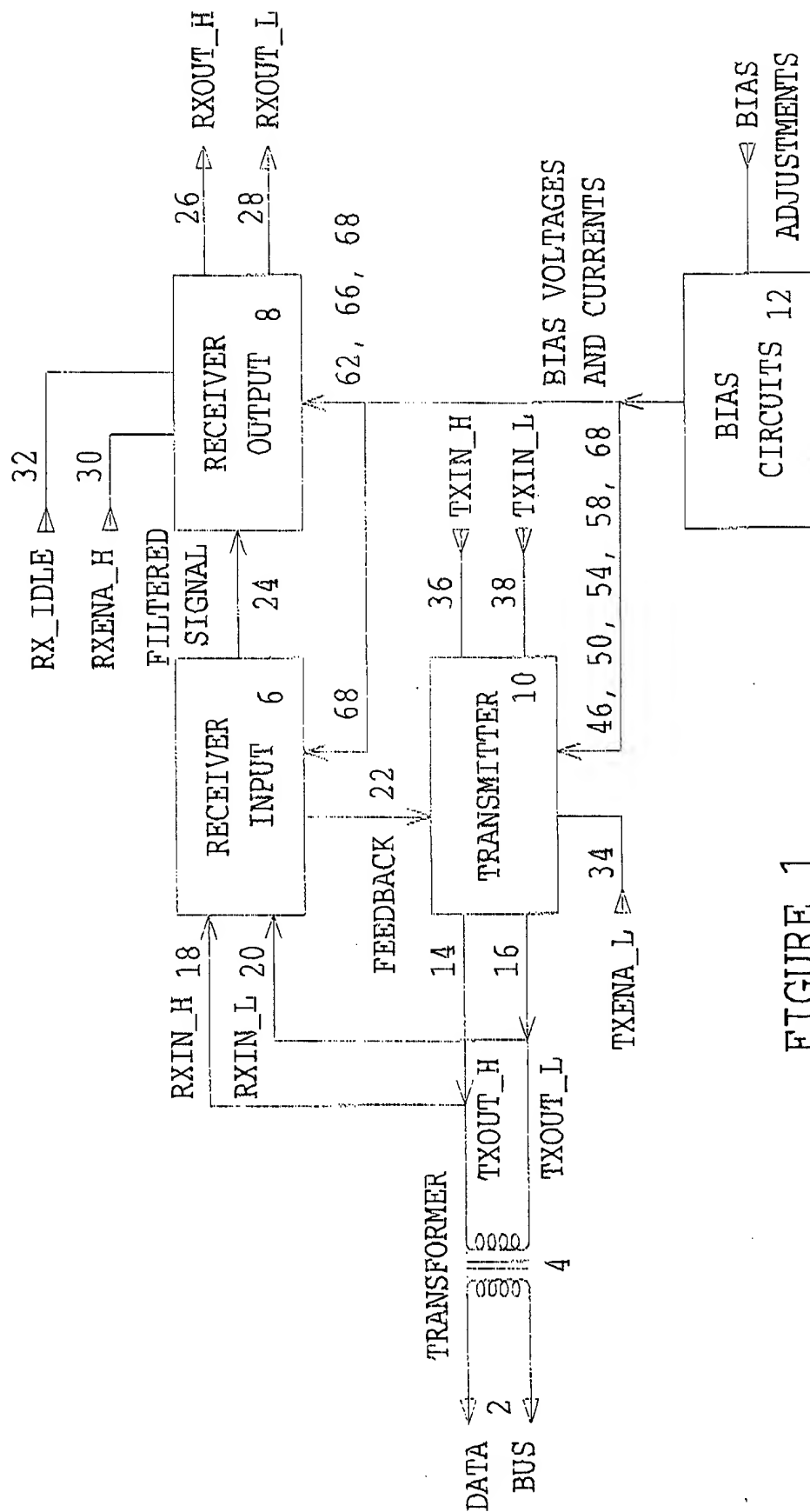


FIGURE 1

40, 42, 44, 48, 52, 56, 60, 64

FIG. 2 is a schematic diagram of a differential amplifier circuit. The circuit includes two input terminals, RXIN_H (18) and RXIN_L (20), each connected to a resistor (206, 208) and a BGREF (68) terminal. The RXIN_H input is connected to the non-inverting input (+) of a first amplifier (200). The RXIN_L input is connected to the inverting input (-) of a second amplifier (202). The outputs of the first and second amplifiers are connected to a common node (212), which is also connected to a BGREF (68) terminal. The common node (212) is connected to a feedback network consisting of a resistor (214) and a capacitor (216). The feedback network is connected to a node (220), which is also connected to a BGREF (68) terminal. The node (220) is connected to a differential pair of transistors (228, 230) and a node (232). The node (232) is connected to a BGREF (68) terminal. The output of the differential pair is connected to a node (222), which is connected to a node (224). The node (224) is connected to a node (226), which is connected to a node (230). The node (230) is connected to a node (232), which is connected to a BGREF (68) terminal. The output of the differential pair is connected to a node (222), which is connected to a node (224). The node (224) is connected to a node (226), which is connected to a node (230). The node (230) is connected to a node (232), which is connected to a BGREF (68) terminal.

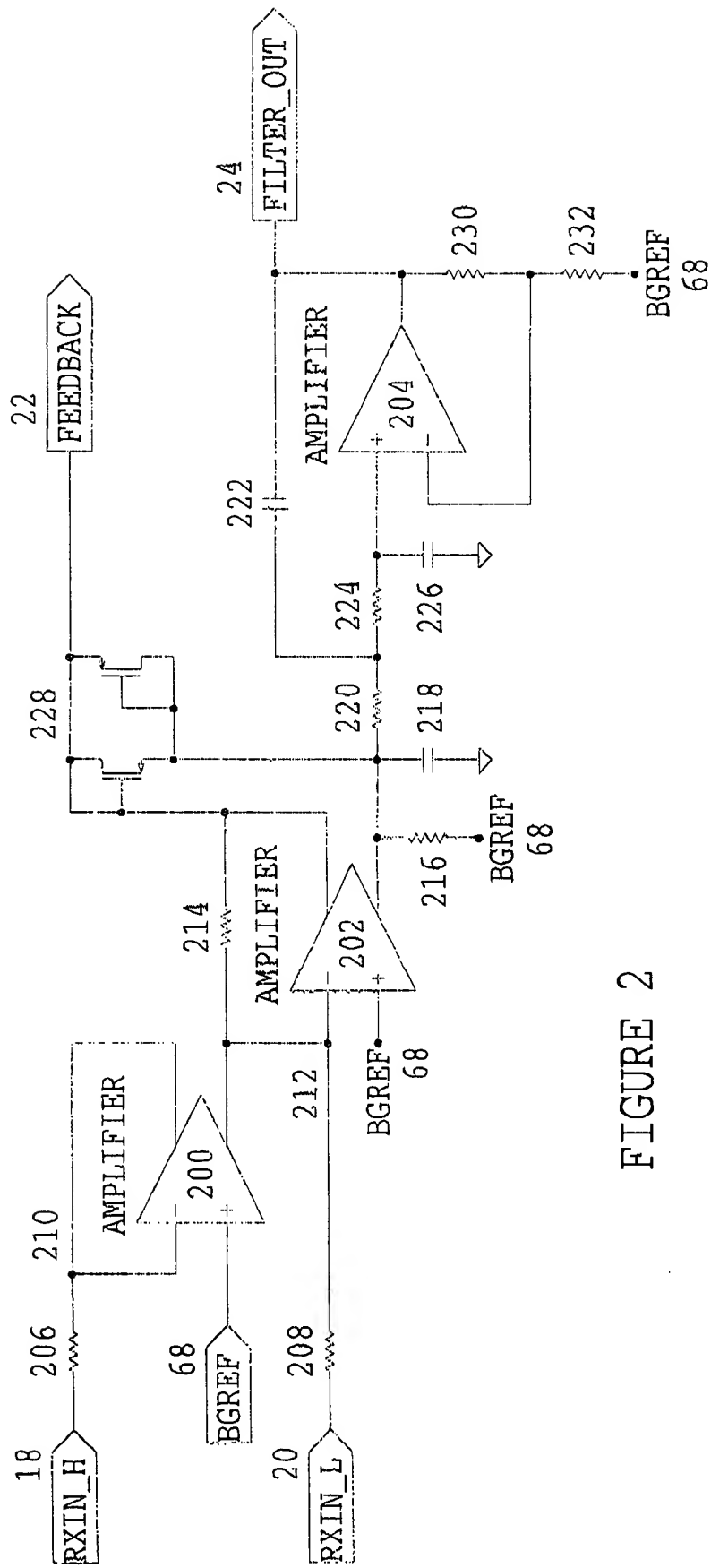


FIGURE 2

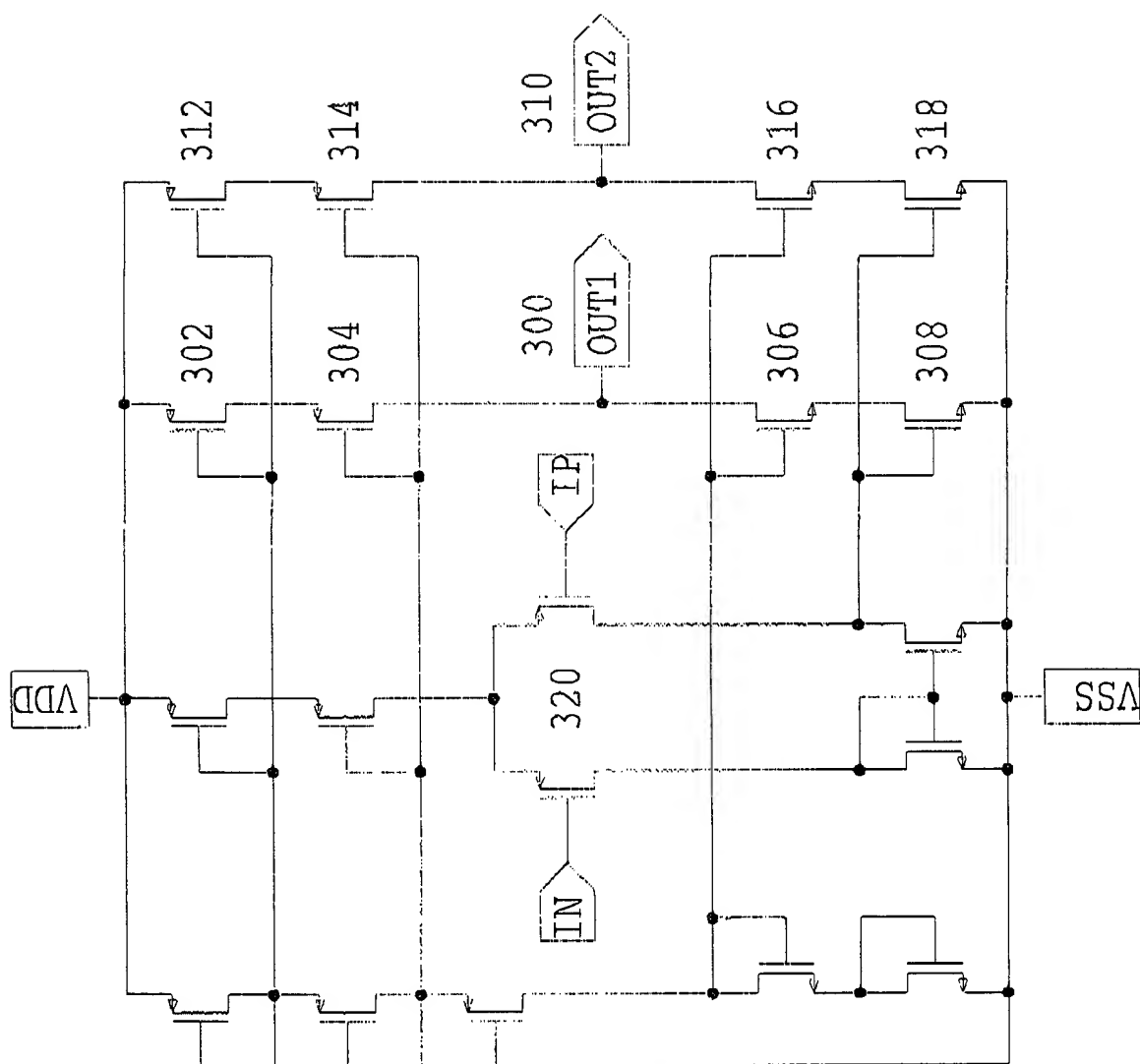


FIGURE 3

FIG. 4 is a block diagram of a receiver circuit 400 in accordance with one embodiment of the present invention. The receiver circuit 400 includes a first comparator 410, a second comparator 414, and a filter circuit 406. The first comparator 410 has a non-inverting input (+) and an inverting input (-). The non-inverting input (+) is connected to a filter output 406, which is the output of a filter circuit 406. The filter circuit 406 has an input 24 and an output 406. The input 24 is connected to a voltage divider network consisting of a resistor 408 and a resistor 406. The voltage divider network is connected to a voltage source 66, which is labeled VTHP. The output 406 of the filter circuit 406 is connected to the non-inverting input (+) of the first comparator 410. The inverting input (-) of the first comparator 410 is connected to a voltage source 62, which is labeled VTHN. The output of the first comparator 410 is connected to a signal line 412, which is labeled NOT_BELOW. The second comparator 414 has a non-inverting input (+) and an inverting input (-). The non-inverting input (+) is connected to a voltage source 68, which is labeled BGRF. The inverting input (-) of the second comparator 414 is connected to a signal line 416, which is labeled NOT_ABOVE. The output of the second comparator 414 is connected to a signal line 414, which is labeled ABOVE_H. The signal line 412 (NOT_BELOW) is connected to an AND gate 422. The signal line 414 (ABOVE_H) is connected to an AND gate 424. The output of AND gate 422 is connected to a signal line 430, which is labeled RX_LOW. The output of AND gate 424 is connected to a signal line 432, which is labeled RX_HIGH. The signal line 430 (RX_LOW) is connected to an ESD protection circuit 434, which is labeled ESD3. The signal line 432 (RX_HIGH) is connected to an ESD protection circuit 436, which is labeled ESD3. The outputs of the ESD protection circuits 434 and 436 are connected to signal lines 28 and 26, respectively, which are labeled RXOUT_L and RXOUT_H. The signal line 430 (RX_LOW) is also connected to an AND gate 438. The signal line 432 (RX_HIGH) is also connected to an AND gate 438. The output of AND gate 438 is connected to a signal line 32, which is labeled RX_IDLE. The signal line 416 (NOT_ABOVE) is connected to an AND gate 426. The output of AND gate 426 is connected to a signal line 428, which is labeled DISABLE. The signal line 428 (DISABLE) is connected to an AND gate 440. The output of AND gate 440 is connected to a signal line 30, which is labeled RXENA_H. The signal line 428 (DISABLE) is also connected to an AND gate 442. The output of AND gate 442 is connected to a signal line 440, which is labeled ENA_L. The signal line 440 (ENA_L) is connected to a signal line 30, which is labeled RXENA_H. The signal line 440 (ENA_L) is also connected to a signal line 442, which is labeled ENA_L. The signal line 442 (ENA_L) is connected to a signal line 30, which is labeled RXENA_H.

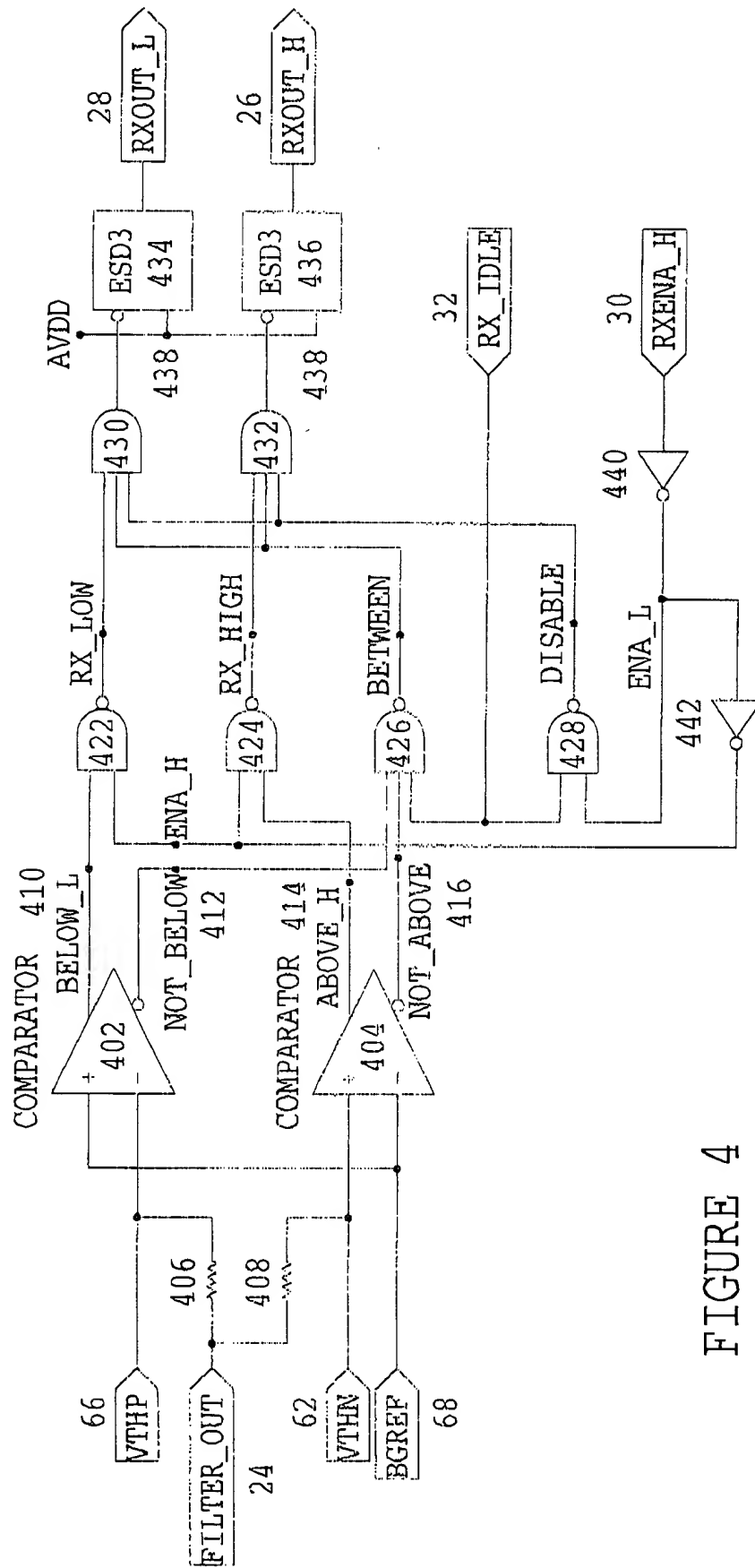


FIGURE 4

FIG. 5 is a schematic diagram of a circuit for generating a pulse width modulated signal.

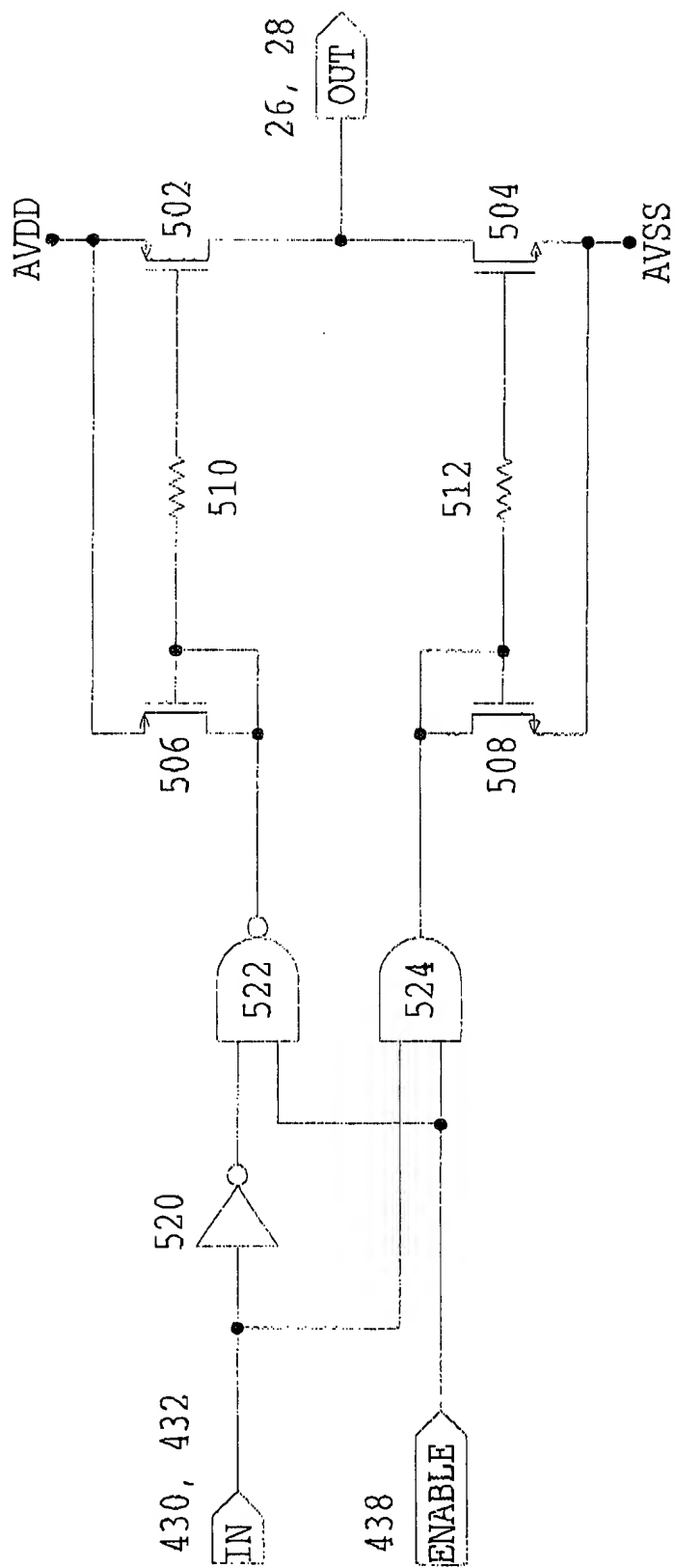


FIGURE 5

FIG. 6 is a schematic diagram of a transmitter circuit in accordance with the present invention.

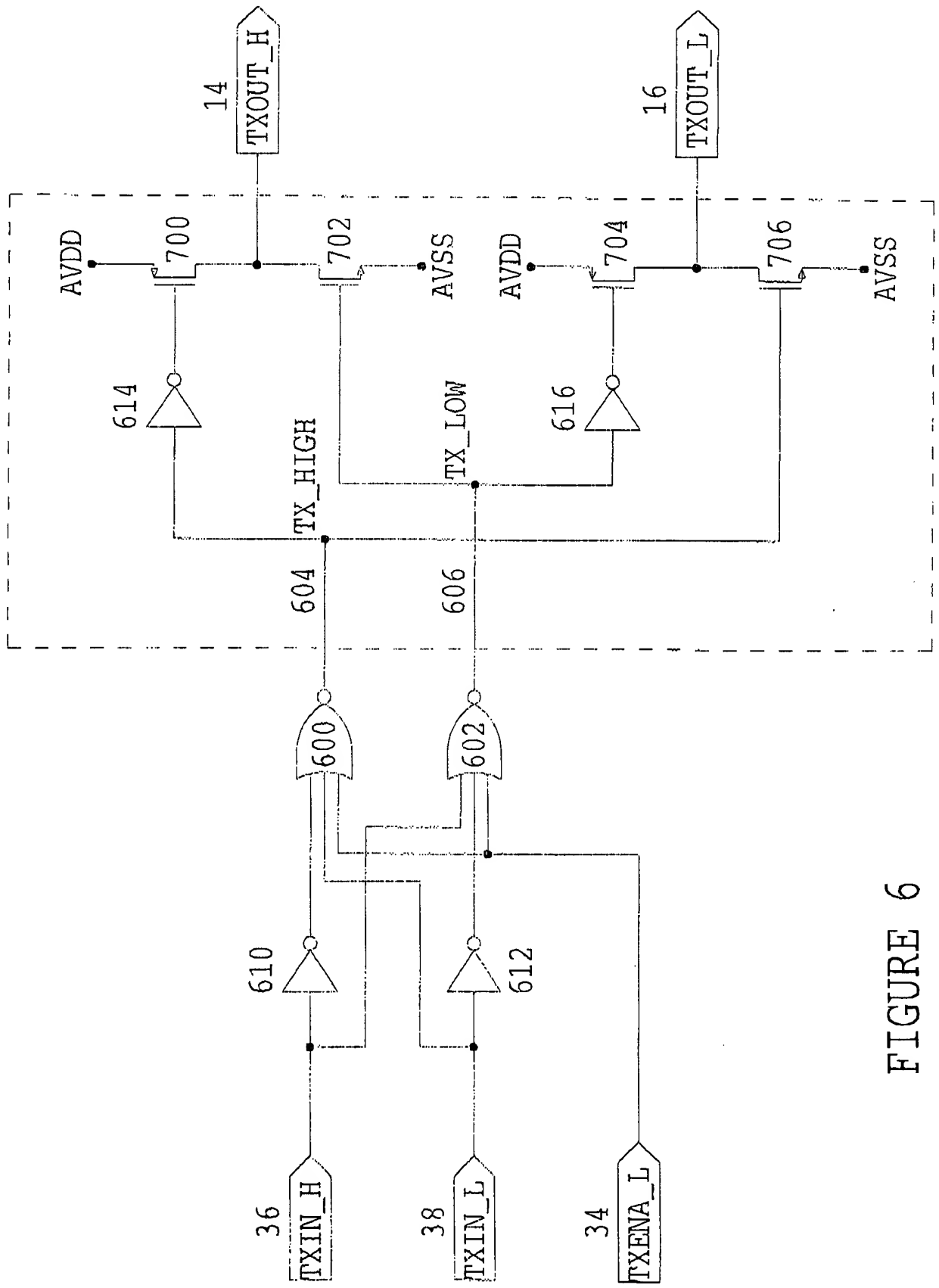


FIGURE 6

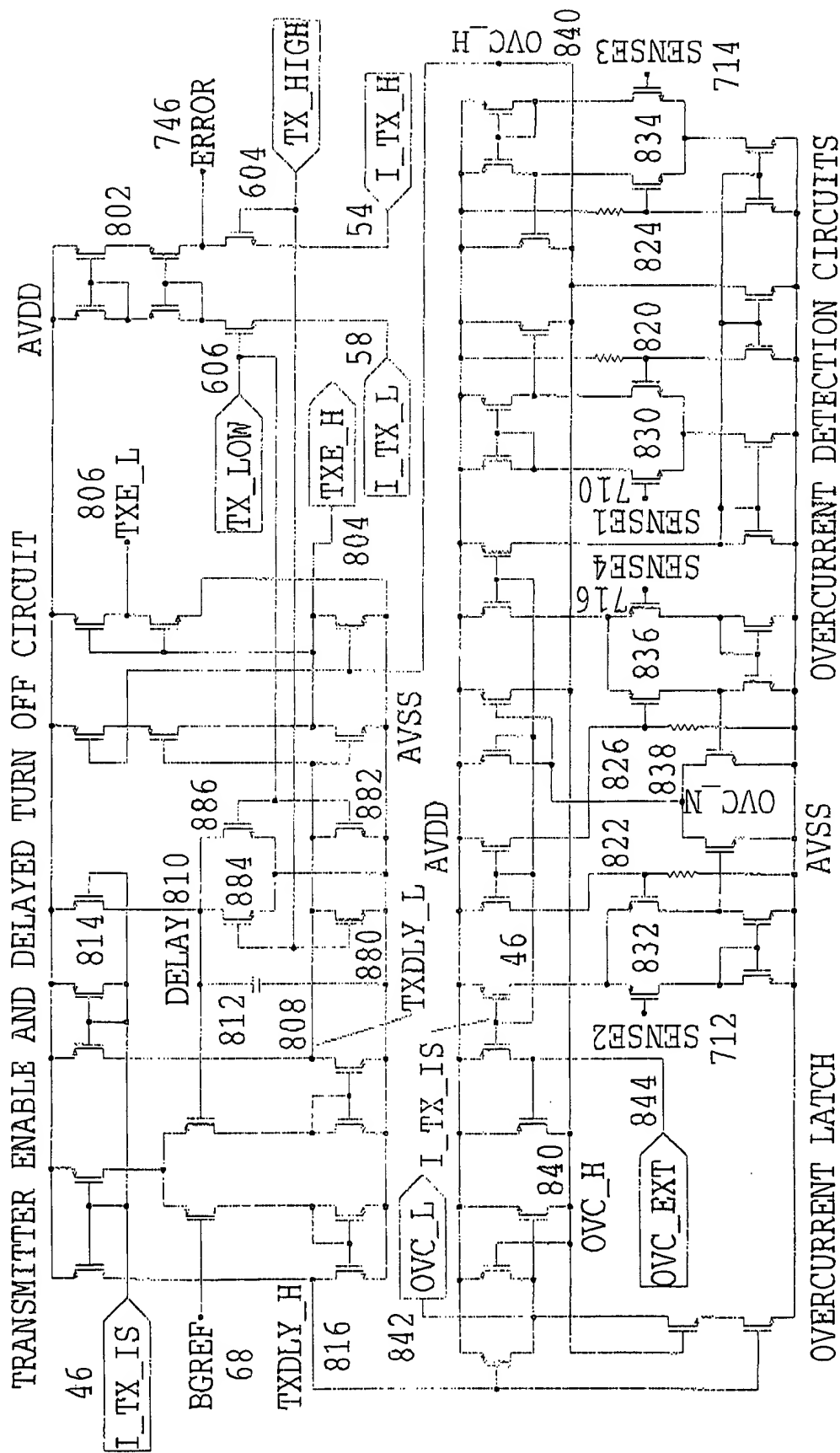


FIGURE 8

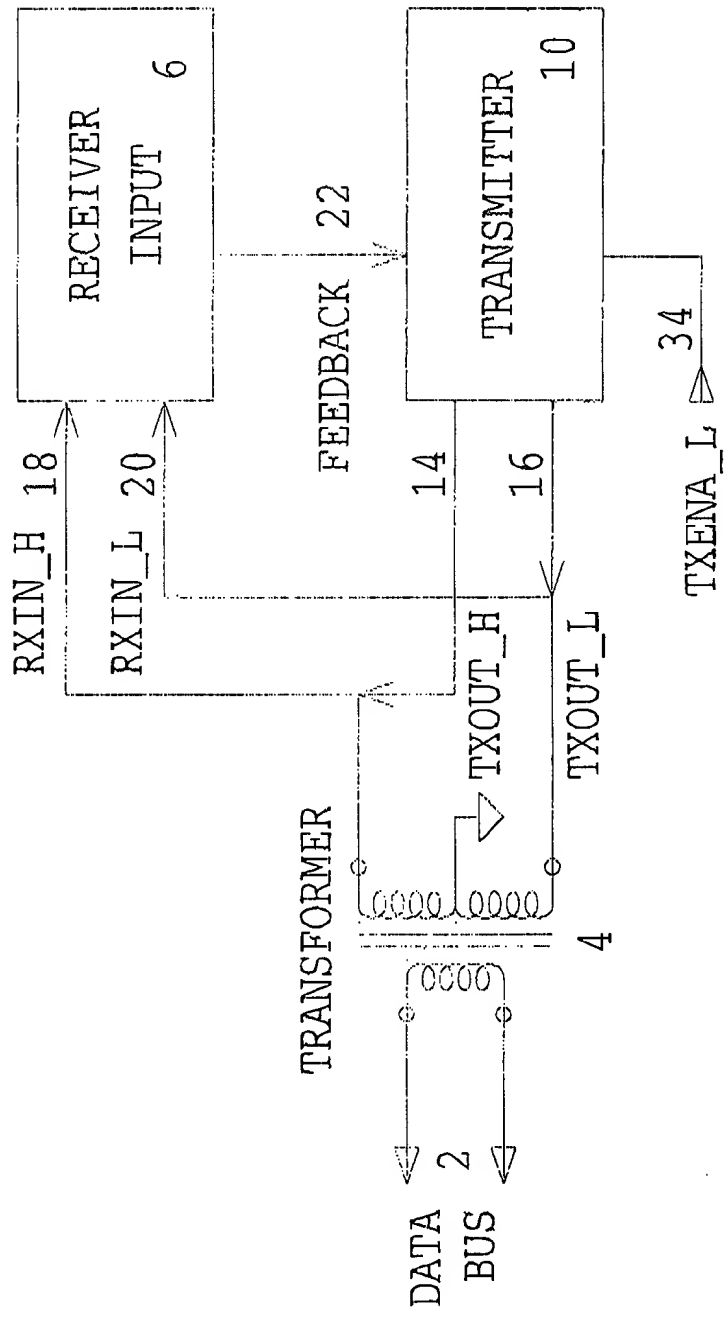


FIGURE 9

When using such a system, the user should be aware of the fact that the system is not a true system and that the system is not a true system.

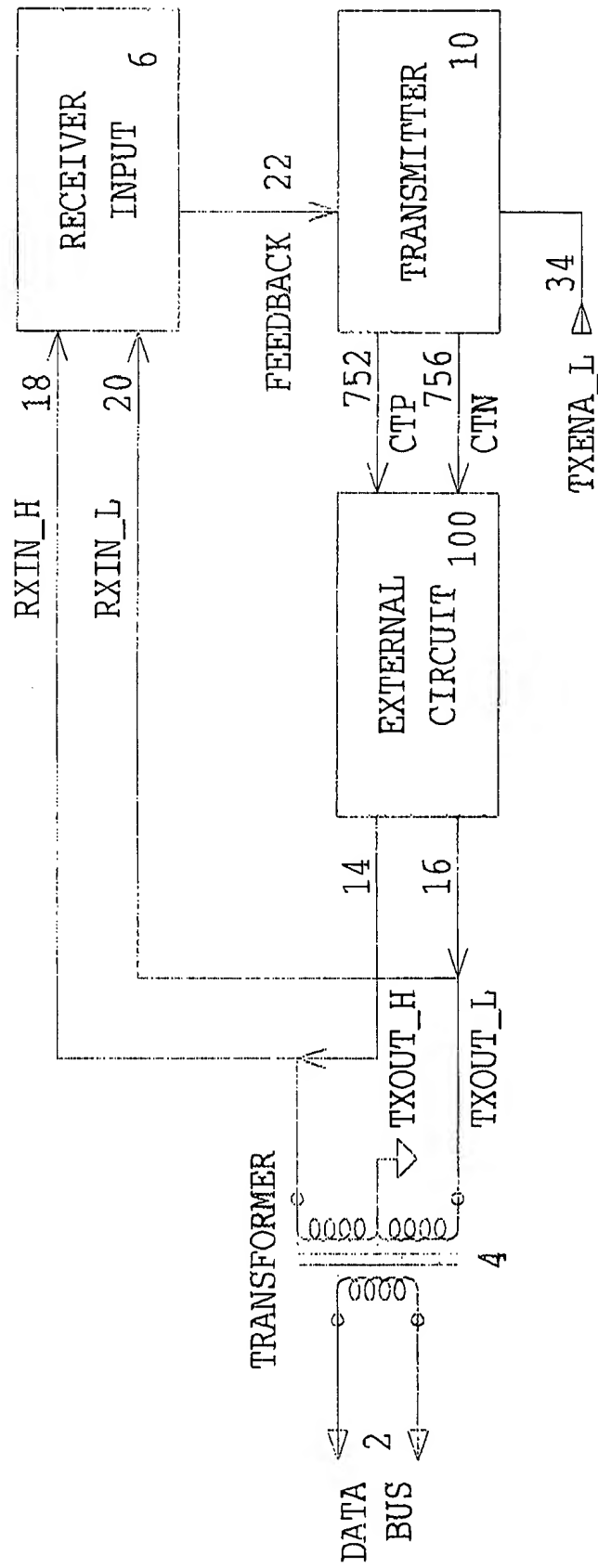


FIGURE 10

FIG. 11 is a schematic diagram of a circuit for generating a differential output signal. The circuit includes a differential pair of transistors 1102 and 1104, a current source 1110, and a load resistor 1106. The circuit is biased by a differential-mode input signal 756 and a common-mode input signal 752. The output signals are TXOUT_H and TXOUT_L. The circuit also includes a feedback loop with a capacitor 1108 and a resistor 1110. The circuit is powered by a VEE supply and an AVSS supply.

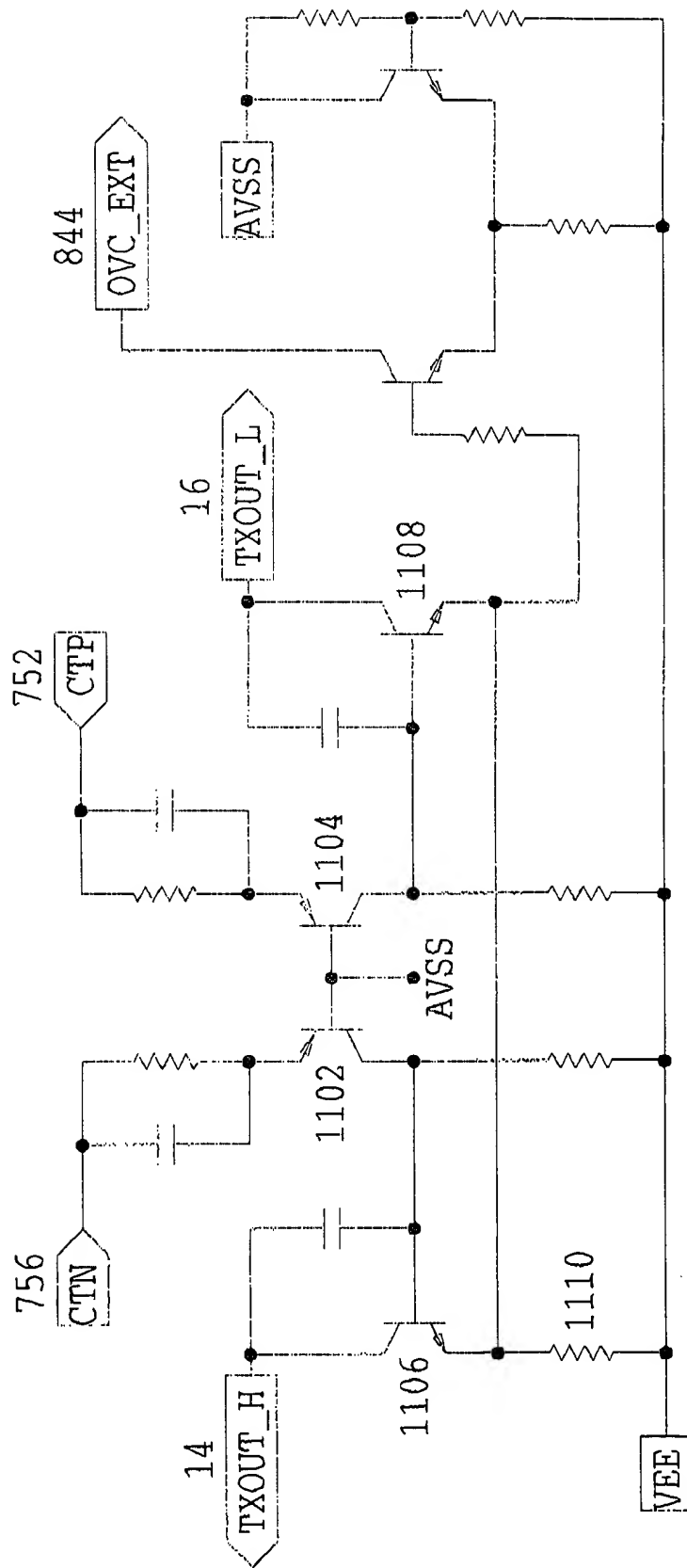


FIGURE 11

FIGURE 12

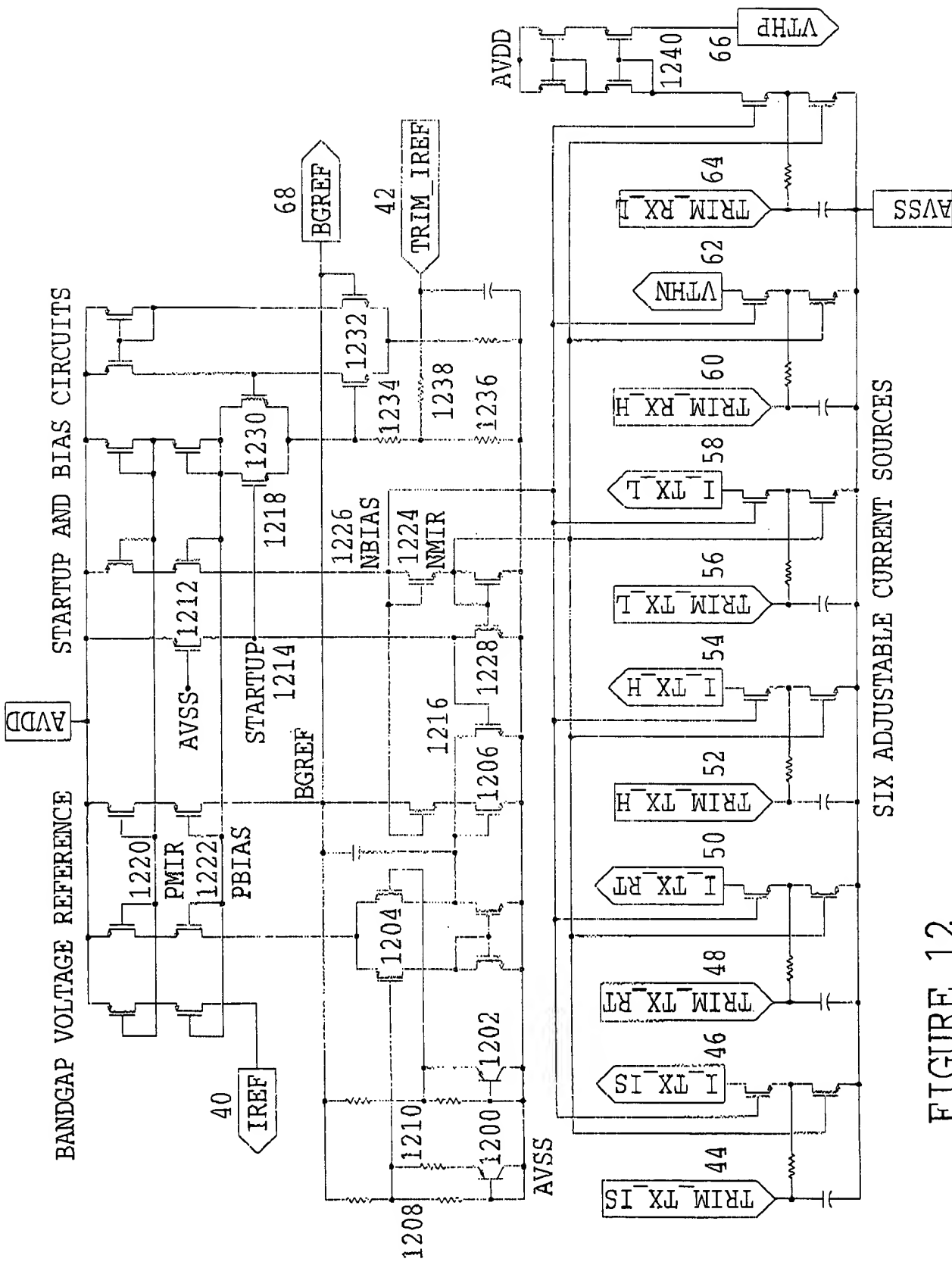


FIGURE 12